PATENT ABSTRACTS OF JAPAN

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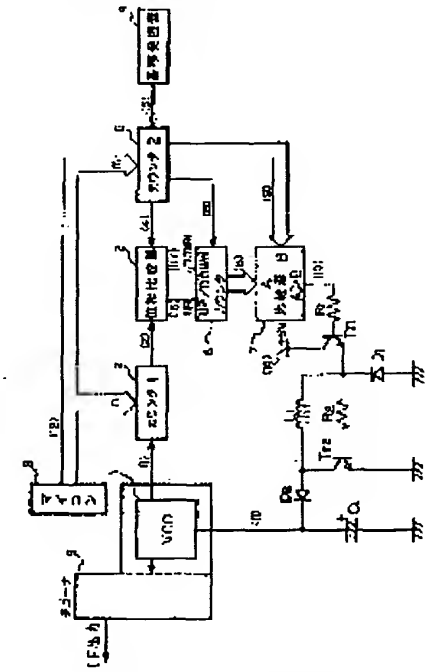
(71)Applicant : SHARP CORP
(72)Inventor : KOJIMA SHIGERU

(54) FREQUENCY DIGITAL SYNTHESIZER SYSTEM TELEVISION RECEIVER

(57)Abstract:
PURPOSE: To reduce switching noise, to miniaturize a transformer and to reduce the rated voltage of parts by constituting a circuit without generating high voltage by a DC/DC converter circuit.
CONSTITUTION: In this digital synthesizer type television receiver, a phase comparator 3 compares a signal 14 obtained by dividing the frequency of a reference signal with a signal 2 obtained by dividing the frequency of an oscillation signal from a VCO 1. A pulse width modulation (PWM) signal is obtained based upon an up/down signal for the control voltage of the VCO 1 obtained by the phase comparator and an objective control voltage signal 11 is obtained by a voltage boosting/dropping circuit.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The television receiver of the frequency digital synthesizer method characterized by to have the counter section which creates rise/down signal of the control voltage of the aforementioned voltage controlled oscillator, and the comparator which create a PDM signal based on the counter output of this counter section in the electronic-equipment equipment which has the frequency digital synthesizer tuner section equipped with the phase comparator which compares a voltage controlled oscillator with the signal which carried out dividing of the reference signal and the signal which carried out dividing of the oscillation signal of the aforementioned voltage controlled oscillator.
[Claim 2] The television receiver of the frequency digital synthesizer method characterized by having a pressor-depressor circuit for ******(ing) reference voltage of the circuit of others of the aforementioned electronic equipment equipment for the control voltage of the aforementioned voltage controlled oscillator in the electronic equipment equipment which has the frequency digital synthesizer tuner section equipped with the phase comparator which compares a voltage controlled oscillator with the signal which carried out dividing of the reference signal and the signal which carried out dividing of the oscillation signal of the aforementioned voltage controlled oscillator.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
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[Industrial Application] this invention relates to the television (TV) receiving set which makes tuning voltage (1-32V) from the low voltage of +5V grade with a pressor-depressor circuit about the television receiver of a frequency digital synthesizer method in the tuning system which used the frequency digital synthesizer method for the detail more.
[0002]
[Description of the Prior Art] ** and the lowered type tuning voltage generating circuit of the former [drawing 4] of the pressure -- it is -- the inside of drawing, and 11 -- a voltage controlled oscillator (Voltage Controlled Oscillator:VCO) and 12 -- for criteria VCO and 15, as for a microcomputer and 17, the 2nd counter and 16 are [the 1st counter and 13 / a phase comparator and 14 / a DC-DC converter and 18] tuners A voltage controlled oscillator (VCO) 11 is controlled by voltage of the voltage signal (11) which determines the oscillation frequency. The 1st counter 12 carries out the output signal (1) of VCO 1/n dividing. A phase comparator 13 compares the phase of the signal (2) which carried out the output signal (1) of VCO 1/n dividing by the 1st counter, and the signal which carried out the normal-output signal 1/m dividing by the 2nd counter. The 2nd counter 15 carries out a reference signal 1/m dividing. TR3, R3, R5, C2, and C5 are the circuits for obtaining the target voltage signal (11) from the signal (13) which rectified the output of the voltage conversion transformer T1 by diode D3 and the capacitor C4.
[0003] The division ratio n which carries out dividing of the signal (1) from VCO and the (fHz) to the 1st counter 12 by the signal (12) from a microcomputer 16 is given, and the 1st counter 12 outputs the signal (2) which carried out the signal (1) 1/n dividing. The division ratio m which carries out dividing of the signal (3) from criteria VCO 15 and the (fHz) to the 2nd counter 15 by the signal (12) from a microcomputer 16 is given, and the 2nd counter 15 outputs the signal (4) which carried out the signal (3) 1/m dividing. At this time, n and m are set up on condition that a formula (1).
f/n=F/m -- Formula (1)
[0004] A phase comparator 13 outputs signal (6) and a signal (7) by comparing the output signal (2) of the 1st counter 12 with the output signal (4) of the 2nd counter 15. Signal (6) and a signal (7) operate like a formula (2), a formula (3), and a formula (4).
They are signal (6) and (7) =H level at the time of a signal (2) > signal (4). -- Formula (2)
They are signal (6) and (7) =L level at the time of a signal (2) < signal (4). -- Formula (3)
They are signal (6) and (7) = high impedance at the time of a signal (2) = signal (4). -- Formula (4)
When a signal (7) is L level, it will be in an OFF state, the charge accumulated at the capacitor C4 is charged by the capacitor C3 through resistance R4, and the potential of a signal (11) goes up a transistor TR3. Moreover, when a signal (7) is H level, a transistor TR3 will be in ON state, it discharges from a capacitor C3 through resistance R3, and potential falls.
[0005] At this time, if the voltage of an input signal (11) goes up, oscillation frequency will go up VCO11, and if voltage falls, oscillation frequency will fall. An oscillation is maintained on the oscillation frequency which VCO11 makes the purpose by the above operation being performed

repeatedly. Moreover, a signal (13) (for example, +33V) is a signal which rectified the output of the voltage conversion transformer T1 controlled by DC-DC converter 17 by diode D3 and the capacitor C4.
[0006]
[Problem(s) to be Solved by the Invention] As mentioned above, in the conventional ** and lowered type tuning voltage generating circuit of the pressure, 33V used as reference voltage (signal 13) must be beforehand prepared in the power circuit. For example, if it is the device of cell operation, it will make from DC-DC converter 17 grade simultaneously with other voltage. Supposing negative voltage (for example, -8V) is in other voltage at this time, the difference of the maximum and the minimum value of the transformer output of DC-DC converter 17 must become also more than 100V, and rating of the parts used for a circuit must be enlarged. Moreover, in order that a switching noise may also become large in proportion to voltage and may press it down, you have to add a circuit. Moreover, the winding ratio of a transformer becomes large and there is a trouble of a transformer being enlarged.
[0007] this invention was made in view of such the actual condition, and it is made to be possible [the circuitry of it], without generating the high voltage in a DC-DC converter circuit, and it aims at offering the television receiver of a frequency digital synthesizer method which attained low-battery-ization of a miniaturization and part rating of the reduction and the transformer of a switching noise.
[0008]
[Means for Solving the Problem] In the electronic equipment equipment which has the frequency digital synthesizer tuner section equipped with the phase comparator which compares (1) voltage controlled oscillator with the signal which carried out dividing of the reference signal and the signal which carried out dividing of the oscillation signal of the aforementioned voltage controlled oscillator in order that this invention may attain the above-mentioned purpose having had the counter section which creates rise/down signal of the control voltage of the aforementioned voltage controlled oscillator, and the comparator which creates a PDM signal based on the counter output of this counter section -- or (2) In the electronic equipment equipment which has the frequency digital synthesizer tuner section equipped with the phase comparator which compares a voltage controlled oscillator with the signal which carried out dividing of the reference signal and the signal which carried out dividing of the oscillation signal of the aforementioned voltage controlled oscillator It is characterized by having a pressor-depressor circuit for ******(ing) reference voltage of the circuit of others of the aforementioned electronic equipment equipment for the control voltage of the aforementioned voltage controlled oscillator.
[0009]
[Function] In the receiver of a digital synthesizer method, a phase comparator compares the signal which carried out dividing of the reference signal, and the signal which carried out dividing of the oscillation signal of VCO, a PWM (PDM) signal is acquired based on rise/down signal of the control voltage of VCO calculated with the phase comparator, and the target control voltage is obtained with a pressor-depressor circuit.
[0010]
[Example] An example is explained below with reference to a drawing. Drawing 1 is a block diagram for explaining television-receiver 1 example of the frequency digital synthesizer method by this invention, and drawing 2 and drawing 3 are drawings showing the signal wave form of each part in drawing 1 . the inside of drawing, and 1 -- a voltage controlled oscillator (VCO) and 2 -- the 1st counter and 3 -- for the 2nd counter and 6, as for a comparator and 8, rise/down (UP/DOWN) counter and 7 are [a phase comparator and 4 / criteria VCO and 5 / a microcomputer and 9] tuners
[0011] A voltage controlled oscillator (VCO) 1 is controlled by the voltage signal (11) which determines the oscillation frequency. The 1st counter 2 carries out a VCO output signal (1) 1/n dividing. A phase comparator 3 compares the phase of the signal (2) which carried out the output signal of VCO 1/n dividing by the 1st counter, and the signal (4) which carried out the reference signal from criteria VCO 1/m dividing by the 2nd counter. The 2nd counter 5 carries out a reference signal 1/m dividing. A up / down counter 6 is risen / downed with the rise signal (16)

of a phase comparator, and the down signal (17) of a phase comparator. A comparator 7 compares the signal (9) which ****(ed) the output signal (8) and reference signal of a up / down counter by the 2nd counter. A microcomputer 8 gives division-ratio n-m to the 1st counter 2 and 2nd counter 5. R1, TR1, D1, L1, R2, TR2, D2, and C1 are circuits which the voltage of the voltage signal (11) which determines the oscillation frequency of VCO is made to ****** by the pulse width of the output signal 10 of a comparator.

[0012] The division ratio n which carries out dividing of the signal (1) from VCO1 and the (fHz) to the 1st counter 2 by the signal (12) from a microcomputer 8 is given, and the 1st counter 2 outputs the signal (2) which carried out the signal (1) 1/n dividing. The division ratio m which carries out dividing of the signal (3) from criteria VCO 4 and the (fHz) to the 2nd counter 5 by the signal (12) from a microcomputer 8 is given, and the 2nd counter 5 outputs the signal (4) which carried out the signal (3) 1/m dividing. At this time, n and m are set up on condition that the above-mentioned formula (1).

f/n=F/m -- Formula (1)

[0013] By comparing the output signal (2) of the 1st counter 2 with the output signal (4) of the 2nd counter 5, a phase comparator 3 outputs signal (16) and a signal (17). Signal (16) and a signal (17) operate like a formula (5), a formula (6), and a formula (7).

It is signal (16) =H level at the time of a signal (2) > signal (4). Signal (17) =L level -- Formula (5)

It is signal (16) =L level at the time of a signal (2) < signal (4). Signal (17) =H level -- Formula (6)

It is signal (16) =L level at the time of a signal (2) = signal (4). Signal (17) =L level -- Formula (7)

[0014] A up / down counter 6 carries out a rise count, when a signal (17) is H level, when a signal (16) is H level, it carries out a down count, and when signal (16) - (17) is both L level, it does not perform a count. Moreover, the count clock signal (5) of this counter is beforehand outputted on fixed frequency from the 2nd counter 5. Namely, the output signal (8) (for example, 8-bit binary data) of a up / down counter 6 is raised at the time of a signal (2) > signal (4), and is downed at the time of a signal (2) < signal (4). The signal (8) outputted from the up / down counter 6 is inputted into a comparator 7, and it is compared with the signal (9) outputted from the 2nd counter 5, and if it is a signal (8) > signal (9), H level will be outputted to a signal (10).

[0015] That is, pulse width t of a signal (10) spreads, when raising the oscillation frequency of VCO1, and when lowering, it narrows. Duty ratio changes with the frequency in which VCO1 oscillates a signal (10) by operation of these series. From the voltage of a signal (14), at the time of a low, the square wave of a signal (10) passes along a transistor TR1, and the voltage of a signal (11) is equalized by the LC filter of L1 and C1, and can obtain the target voltage. At this time, a transistor TR2 will not be in an active state. If the square wave of a signal (10) turns on a transistor TR1 when the voltage of a signal (11) is higher than the voltage of a signal (14), a transistor TR2 is also turned on and energy is stored in L1, and at the time of OFF, this energy can be made to be able to superimpose on input voltage, and it can pass along diode D2, and can take out to a capacitor C1, and the target voltage can be obtained. At this time, if the voltage of an input signal (11) goes up, oscillation frequency will go up VCO1, and if voltage falls, oscillation frequency will fall. Thus, with the made signal (11), VCO1 oscillates the target frequency. A special high voltage like a signal (13) is not used, but a signal (11) is acquired from the low battery (for example, +5V) which surely exists in these systems using a pressor-depressor circuit.

[0016]

[Effect of the Invention] According to this invention, there are the following effects so that clearly from the above explanation.

(1) Since composition of a circuit can be performed without generating the high voltage in a DC-DC converter circuit, in the conventional circuit, an effect is in low-battery-ization of a miniaturization and part rating of the reduction and the transformer of the switching noise which was a problem, and a miniaturization and cost cut of a circuit can be aimed at.

(2) Use the output of the phase comparator of a frequency synthesizer, give the concrete variation from the present VCO frequency in the up / down counter of the next step from the signal of whether frequency is raised or to lower, and output the PDM signal proportional to VCO frequency to control by the comparator. It is not necessary to prepare a filter outside in an

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(2) Use the output of the phase comparator of a frequency synthesizer, give the concrete variation from the present VCO frequency in the up / down counter of the next step from the signal of whether frequency is raised or to lower, and output the PDM signal proportional to VCO frequency to control by the comparator. It is not necessary to prepare a filter outside in an

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is a block diagram for explaining one example of the television receiver of the frequency digital synthesizer method by this invention.
[Drawing 2] It is drawing (the 1) showing the signal wave form of each part in drawing 1 .
[Drawing 3] It is drawing (the 2) showing the signal wave form of each part in drawing 1 .
[Drawing 4] It is the block diagram of the television receiver of the conventional frequency digital synthesizer method.
[Description of Notations]
1 [-- A phase comparator, 4 / -- Criteria VCO, 5 / -- The 2nd counter, 6 / -- A up / down counter, 7 / -- A comparator, 8 / -- A microcomputer, 9 / -- Tuner.] -- A voltage controlled oscillator (VCO), 2 -- The 1st counter, 3

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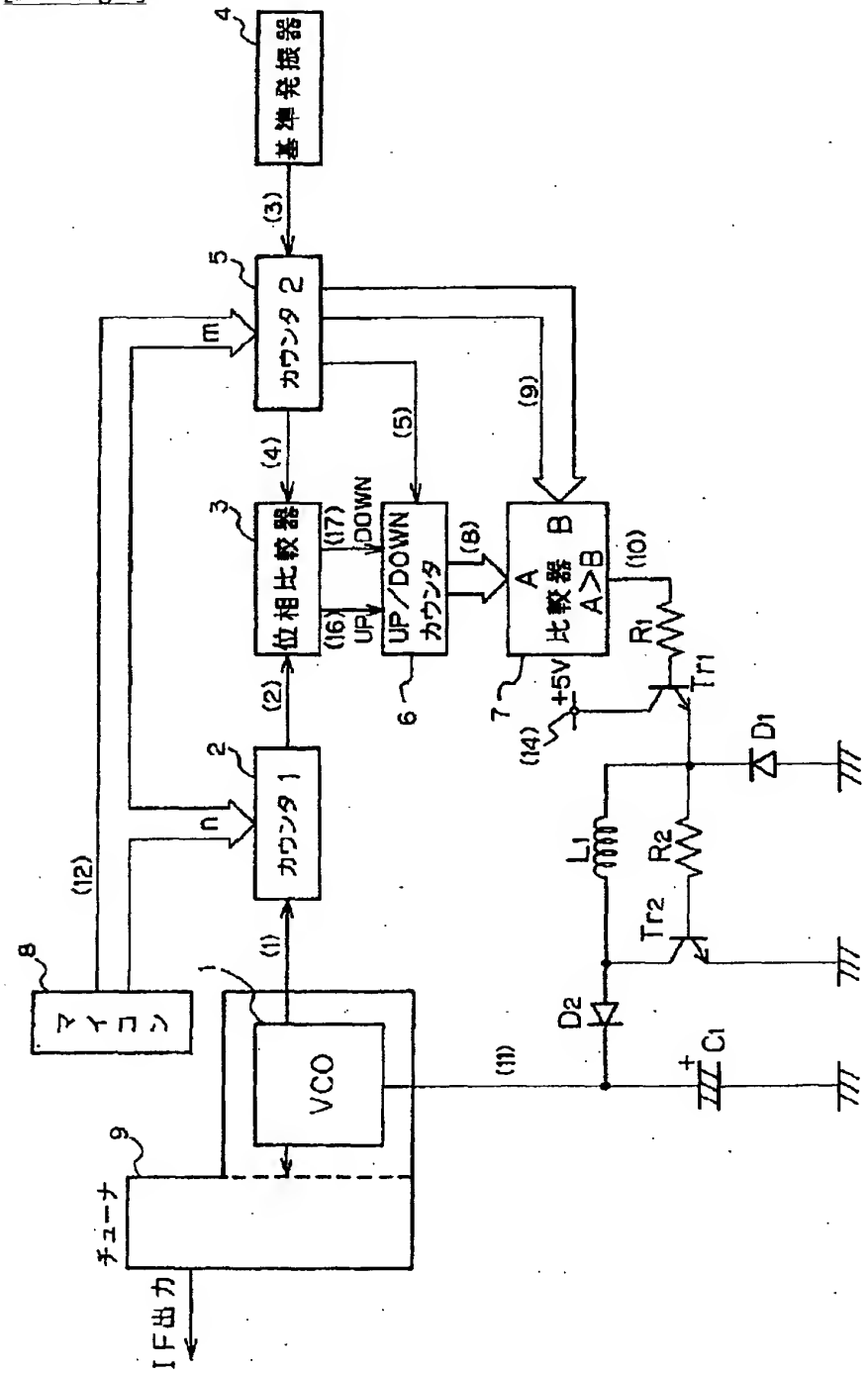
DRAWINGS

[Drawing 1]



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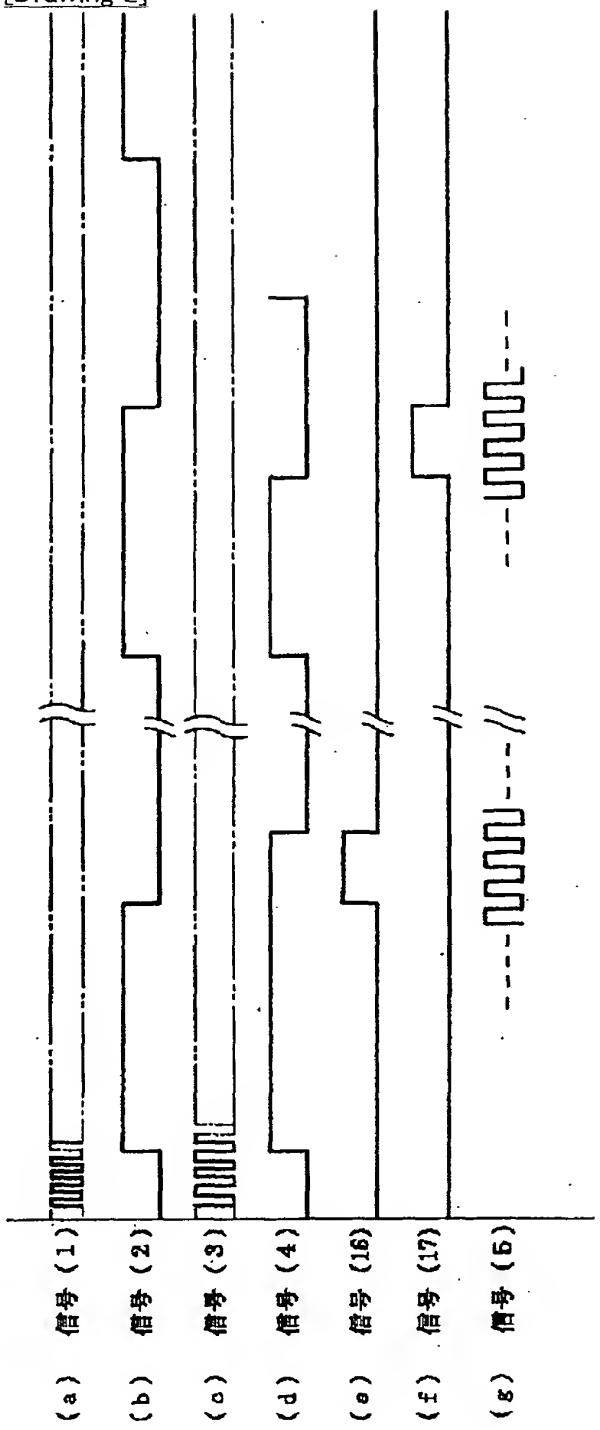
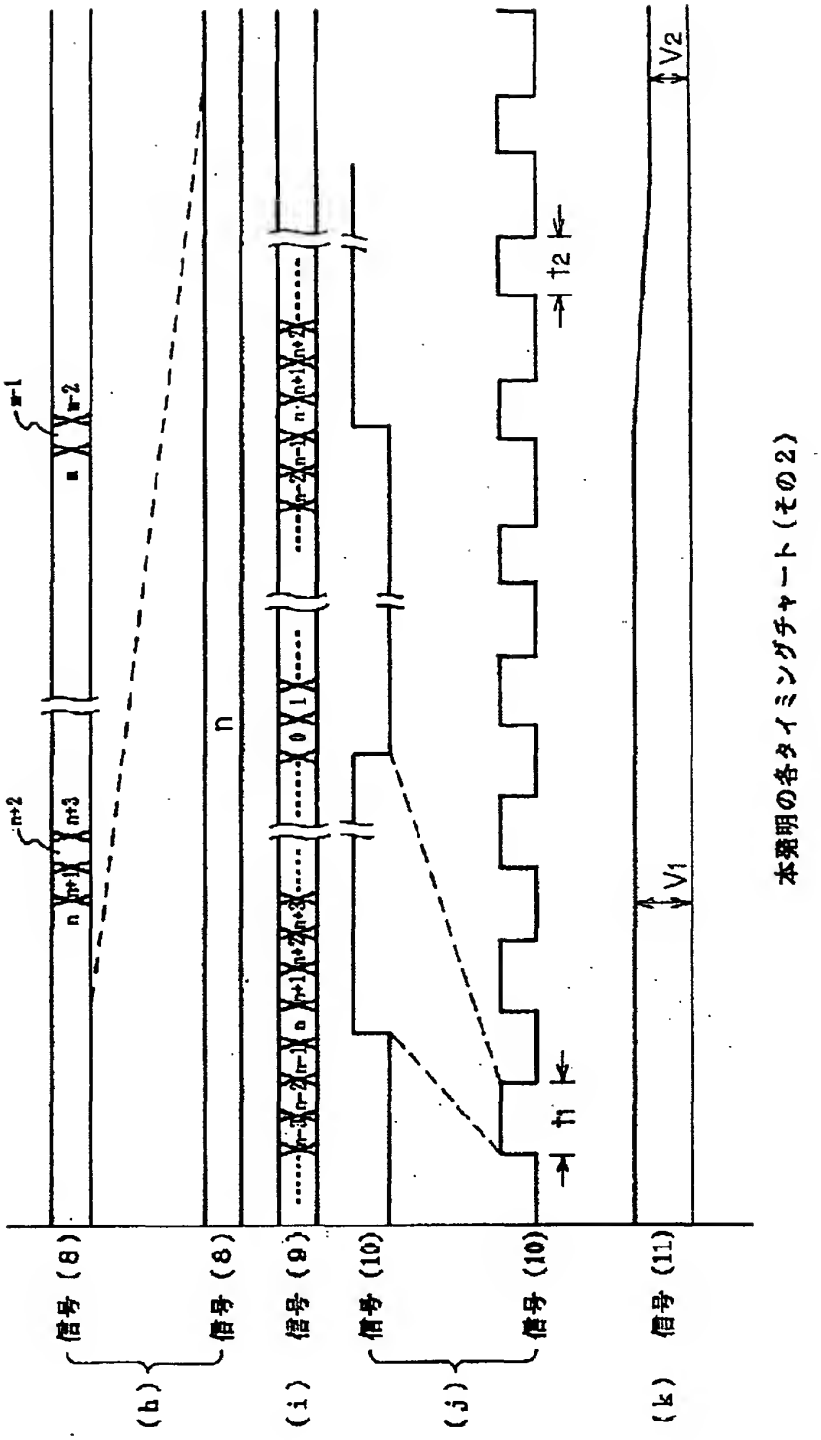


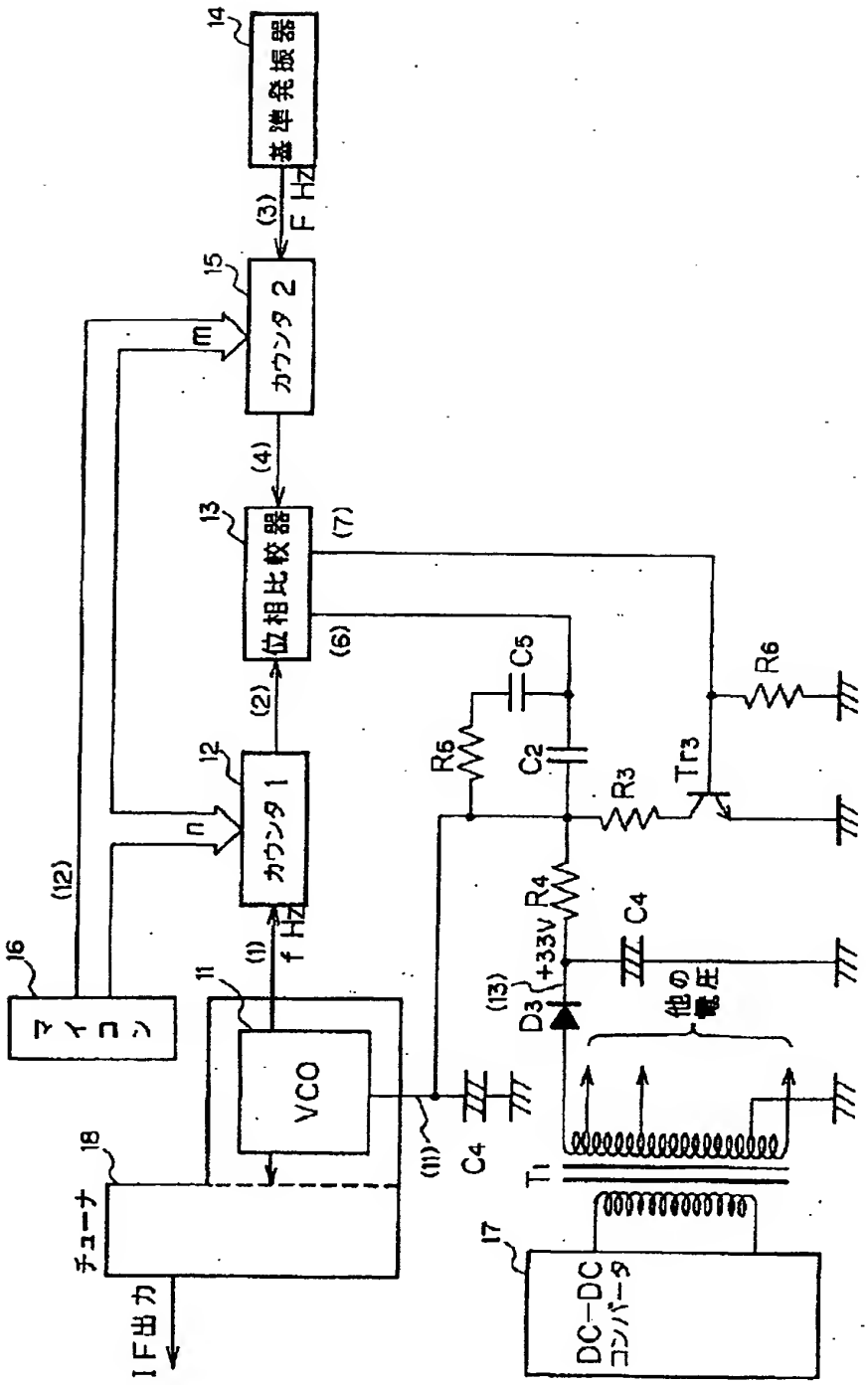
本発明の各タイミングチャート（その1）

[Drawing 3]



本発明の各タイミングチャート（その2）

[Drawing 4]



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